AVR32110: Using the AVR32 Timer/Counter

Features

- **Three independent 16 bit Timer/Counter Channels**
- **Multiple uses:**
  - **Waveform generation**
  - **Analysis and measurement support:**
    - **Frequency and interval measurements**
    - **Event counting**
  - **Pulse Width Modulation**
- **Highly configurable**
  - **3 external clock inputs, 5 internal clock inputs**
  - **Two multi-purpose I/O channels**
- **Internal interrupt support**

1 Introduction

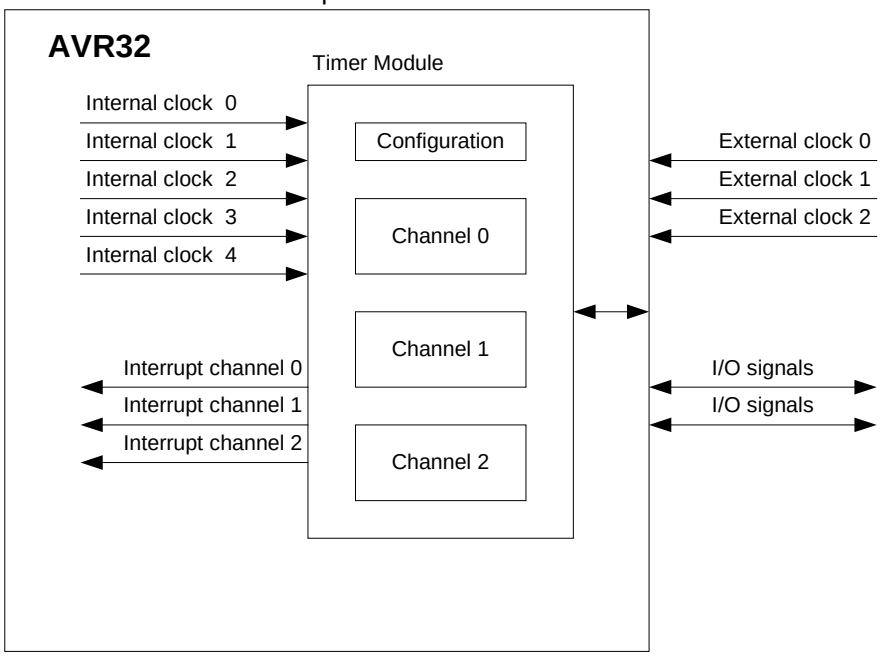
The Timer/Counter Module in the AVR®32 consists of 3 identical and independent channels. These channels can be programmed independently of each other to support frequency measurement, event counting, pulse generation, pulse width modulation, among other features. 8 different clock sources can be used. There is an interrupt for each channel, which can be programmed to enable processor interrupts. There is a Block Control register that can start all three channels simultaneously.

32-bit AVR® Microcontrollers

Application Note

Rev. 32012A-AVR32-05/06

Figure 1: Timer/Counter Conceptual Schematics



2 Theory of operation

2.1 Overview

The Timer/Counter Module has 3 independent timers, which can be individually configured. These three timers can be configured to tick with the same frequency of one out of 8 potential clock sources. Five of these sources are internal, while 3 are external. These counters are 16-bit.

In addition, the Timer/Counter Module is a multi-purpose module for signal generation, signal capture and event counting. There are two distinct modes:

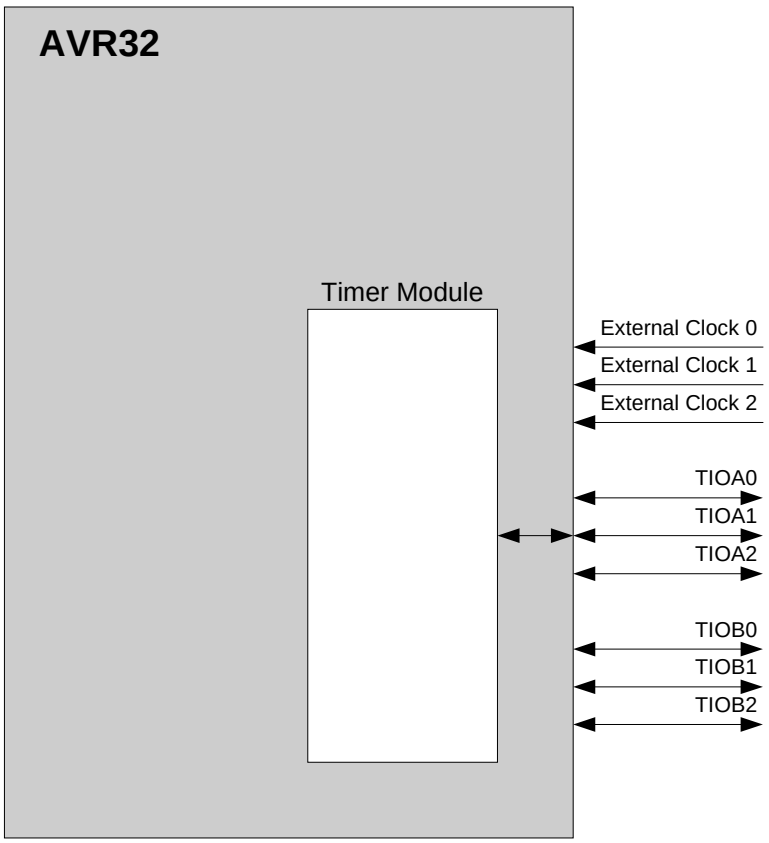
- Waveform mode
- Capture Mode

By selecting the Waveform Mode, signals can be generated on the output, while the Capture Mode reads an input and analyzes it according to the settings.

2.2 I/O Connectivity

There are 3 external clock sources that can be connected to the Timer/Counter Module. In addition there are two signals named TIOA and TIOB for each of the three channels. I.e. the TIOB signal for channel 2 is named TIOB2. Conceptual schematic of this is shown in Figure 2.1.

Figure 2.1: I/O schematics



2.3 Counting

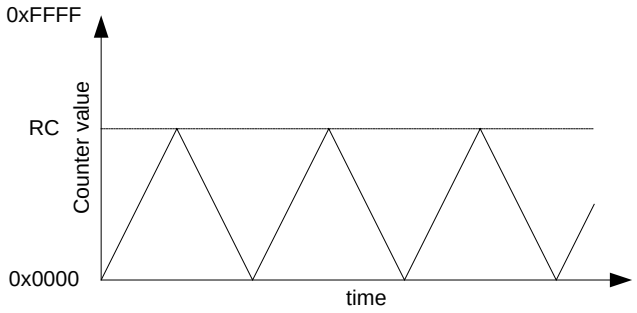
One of the 8 available clock sources is used as a reference for any given timer. These counters will overflow at 0xFFFF. The behavior of each individual counter can be configured in one out of four ways:

- Up Mode: Whenever the counter reaches 0xFFFF, it will reset and restart from 0x0000.
- Up/Down Mode: Whenever the counter overflows at 0xFFFF, it will start counting in the opposite direction. I.e. when the counter reaches 0xFFFF it will count down towards 0x0000.
- Up Mode with Trigger: A compare register may be set to a specific value. When the counter reaches this value, it will restart from 0x0000.
- Up/Down Mode with Trigger. A compare register may be set to a specific value. When the counter reaches this value, it will start counting downwards.

An example of a configuration mode is shown in Figure 2.2. Here a specific trigger value is set and Up/Down Mode with Trigger is selected. This trigger is stored in a

register named RC. The counter value will start counting, and alter direction whenever the trigger value or 0x0000 is reached.

Figure 2.2: Up/Down Mode with Trigger

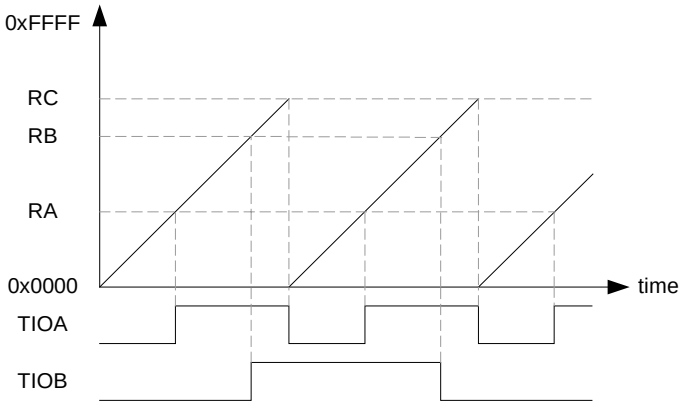


2.4 Waveform Mode

To generate a waveform two additional compare registers are used, namely RA and RB. These registers will neither reset the counter nor reverse the direction, but they can be programmed to trigger an event whenever the counter reaches the actual value; i.e. drive the TIOA line low. The RC trigger works on both I/O lines, while the RA works on the TIOA line and the RB operates on the TIOB line. Specific signals can be configured by first configuring a clock source, then the period can be set by using the RC register. The two I/O lines for the channel can be setup to trigger on the RA and RB registers. In Figure 2.3 a timer is set up to use the Up Mode with Trigger. The RA, RB and RC registers are set with increasing values. The TIOA line is configured so that it sets the line high when RA is reached and clears the line when RC is reached. The TIOB line is set to toggle the line whenever RB is reached.

By using these registers and set up the events properly, complex waveforms can be generated.

Figure 2.3: Waveform Mode using Up Mode with Trigger



As shown in Figure 2.3, complex signals can be generated. The pulses on TIOA or TIOB can i.e. be used as PWM-signals, or other control signals may be implemented.

2.5 Capture Mode

Instead of writing to a channel, the channel can be used for analyzing incoming signals or waveforms. Both I/O channels (TIOA & TIOB) can be used for this. A timer is set up in the same way as for Waveform Mode, with a clock source and with and RC trigger if needed. Then each channel can be setup individually to trig on rising, falling or both edges for TIOA or TIOB, independently of each other. Whenever the line triggers, the channel TC is stored in either RA or RB for TIOA or TIOB respectively. Further analysis can then be made of the input waveform.

2.6 Interrupts

The Timer/Counter Module has support for interrupts. The following interrupts are available for each channel:

- Counter overflow
- Load overflow
- Compare interrupt for RA, RB and RC
- Load interrupt for RA and RB
- External trigger

This interrupts can be utilized by setting up interrupt handlers. Consult application note AVR32101 for details on how to setup and utilize interrupt handlers.

3 User interface

The Timer/Counter Mode user interface is divided into global Timer/Counter settings and settings specific for each individual channel. All registers have a reset value of 0. Register base addresses are found in the datasheet for your specific device.

3.1 Global Settings

These settings are applied to each Timer/Counter instance available on your specific part. There are two registers; one for synchronizing the channels and one for selection of clock source.

3.1.1 Block Control Register

The Block Control Register (BCR) consists of a single bit, called SYNC. If asserted, this bit asserts a software trigger to all channels simultaneously. This register is write-only.

3.1.2 Block Mode Register

This register chooses one of the external clock sources for the Timer/ Counter Module instance. The 6 least significant bits of the register is used for this. This register is a read/write register.

Table 1: 8 LSBs of BMR

7	6	5	4	3	2	1	0
-	-	TX2XC2S		TX1XC1S		TX0XS0S	

Each of the 3 bit fields may have the following values for TX0XS0S:

Table 2: External clock Signal 0 selection

TX0XC0S		Signal connected to XC0
0	0	TCLK0
0	1	None
1	0	TIOA1
1	1	TIOA2

The same scheme shown in Table 2 applies for TX1XS1S and TX2XS2S.

3.2 Channel specific settings

For each channel there are a series of registers that are customizable. These registers are described in this section.

3.2.1 Channel Control Register

The Channel Control Register (CCR) gives the opportunity to disable and enable clocks, and to apply a software trigger on the specific channel. Only the 3 LSBs are used in this register.

	7	6	5	4	3	2	1	0
	-	-				SWTRG	CLKDIS	CLKEN

- CLKEN – Enables the clock if set.
- CLDIS – Disables the clock if set.
- SWTRG – Asserts a software trigger if set.

3.2.2 Channel Mode Register

This register can have to different mappings; one for Capture Mode and one for Waveform Mode. The mapping depends on the bit named WAVE found in this register. If the WAVE bit is set, the mapping for Waveform Mode is used. If not set, the register mapping for Capture Mode is used. This register is read/write independent of the mapping for each mode.

3.2.2.1 Channel Mode Register: Capture Mode

If Capture Mode is set, the Channel Mode Register has the mapping shown in Table 3. Please note that bit 15 must be cleared to select Capture Mode.

Table 3: Channel Mode Register: Capture Mode

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
-	-	-	-	LDRB		LDRA	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WAVE=0	CPCTRG	-	-	-	ABETRG	ETRGEDG	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LBDIS	LDBSTOP	BURST		CLKI	TCCLKS		

The bits and bit fields have the following description:

- TCCLKS – Timer Counter Clock Select

TCCLKS			Selected Clock
0	0	0	TIMER_CLOCK1 *(internal)*
0	0	1	TIMER_CLOCK2 *(internal)*
0	1	0	TIMER_CLOCK3 *(internal)*
0	1	1	TIMER_CLOCK4 *(internal)*
1	0	0	TIMER_CLOCK5 *(internal)*
1	0	1	XC0 *(external)*
1	1	0	XC1 *(external)*
1	1	1	XC2 *(external)*

- CLKI – Inverts the clock for the timer if set
- BURST

BURST		
0	0	The clock is unaltered
0	1	XC0 is ANDed with the selected clock
1	0	XC1 is ANDed with the selected clock
1	1	XC2 is ANDed with the selected clock

- LDBSTOP – Stops the clock when RB load occurs if set.
- LDBDIS – Disables the clock when RB load occurs if set.
- ETRGEDG – Specifies the edge which external triggers acts upon

ETRGEDG		
0	0	None
0	1	Rising edge
1	0	Falling edge
1	1	Each edge

- EBETRG - If set, uses TIOA as external trigger. Uses TIOB if cleared
- CPCTRG - Resets and starts the counter clock if set.
- WAVE - Set to 0 to enable Capture Mode.
- LDRA - RA Loading Selection

LDRA		
0	0	None
0	1	Rising edge of TIOA
1	0	Falling edge of TIOA
1	1	Each edge of TIOA

- LDRB - RB Loading Selection

LDRB		
0	0	None
0	1	Rising edge of TIOA
1	0	Falling edge of TIOA
1	1	Each edge of TIOA

3.2.2.2 Channel Mode Register: Waveform Mode

When the WAVE bit in CMR is set, then the Waveform Mode register mapping is used.

Table 4: Channel Mode Register: Waveform Mode

31	30	29	28	27	26	25	24
BSWTRG		BEEVT		BCPC		BCPB	
23	22	21	20	19	18	17	16
ASWTRG		AEEVT		ACPC		ACPA	
15	14	13	12	11	10	9	8
WAVE=1	WAVSEL		ENETRG	EEVT		EEVTEDG	
7	6	5	4	3	2	1	0
CPCDIS	CPCSTOP	BURST		CLKI	TCCLKS		

The bits and bit fields have the following description:

- TCCLKS– Timer Counter Clock Select

TCCLKS			Selected Clock
0	0	0	TIMER_CLOCK1 *(internal)*
0	0	1	TIMER_CLOCK2 *(internal)*
0	1	0	TIMER_CLOCK3 *(internal)*
0	1	1	TIMER_CLOCK4 *(internal)*
1	0	0	TIMER_CLOCK5 *(internal)*
1	0	1	XC0 *(external)*
1	1	0	XC1 *(external)*
1	1	1	XC2 *(external)*

- CLKI – Inverts the clock for the timer if set.
- BURST – Disable or enable clock burst.

BURST		
0	0	The clock is unaltered
0	1	XC0 is ANDed with the selected clock
1	0	XC1 is ANDed with the selected clock
1	1	XC2 is ANDed with the selected clock

- CPCSTOP – Stops the clock when RC is reached if set.
- CPCDIS – Disables the clock when RC is reached if set.
- EEVTEDG – Specify which edge to monitor for external events.

EEVTEDG		
0	0	None
0	1	Rising edge
1	0	Falling edge
1	1	Each edge

- EEVT – Select external event source.

EEVT		Signal	TIOB
0	0	TIOB	Input (no generation is possible)
0	1	XC0	Output
1	0	XC1	Output
1	1	XC2	Output

- ENETRG - If set, an external event will reset and start the counter clock.
- WAVSEL – Selects the waveform. Consult chapter 2.4 for more information.

WAVSEL		Effect
0	0	Up mode
0	1	Up mode with automatic trigger on RC Compare
1	0	Up/down mode
1	1	Up/down mode with automatic trigger on RC Compare

- WAVE – Set to enable Waveform Mode.
- ACPA - RA compare effect on TIOA.
- ACPC – RC compare effect on TIOA.
- AEEVT – External event effect on TIOA.
- ASWTRG – Software trigger effect on TIOA.
- BCPB - RB compare effect on TIOB.
- BCPC – RC compare effect on TIOB.
- BEEVT – External event effect on TIOB.
- BSWTRG – Software trigger effect on TIOB.

The bit fields ACPA, ACPC, AEEVT, ASWTRG, BCPB, BCPC, BEEVT and BSWTRG all have the same function:

Register		Effect
0	0	None
0	1	Set
1	0	Clear
1	1	Toggle

3.2.3 Counter Value Register

The Counter Value Register (CV) has a 16-bit read-only bit field labeled CV. This bitfield contains the current value of the timer for the actual channel.

3.2.4 Register A

Register A (RA) is read-only while in Capture Mode, and is read/write if currently running in Waveform Mode. RA contains the current value.

3.2.5 Register B

Register B (RB) is read-only while in Capture Mode, and is read/write if currently running in Waveform Mode. RB contains the current value.

3.2.6 Register C

Register C (RC) is always read/write. RC contains the current value.

3.3 Interrupts

There are three registers associated with interrupts: an enable register, a disable register and a mask register. These registers are independent for each channel.

3.3.1 Interrupt Enable Register

Each bit in the Interrupt Enable Register (IER) may enable an individual interrupt source. This is done by setting the corresponding bit in this register. This register is write-only.

Table 5: IER register mapping

7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

- COVFS – Enable Counter Overflow Interrupt
- LOVRS - Enable Load Overrun Interrupt
- CPAS – Enable RA Compare Interrupt
- CPBS – Enable RB Compare Interrupt
- CPCS – Enable RC Compare Interrupt
- LDRAS – Enable RA Loading Interrupt
- LDRBS – Enable RB Loading Interrupt
- ETRGS – Enable External Trigger Interrupt

3.3.2 Interrupt Disable Register

Each bit in the Interrupt Disable Register (IDR) may disable an individual interrupt source. This is done by setting the corresponding bit in this register. Please note that some of the functionality is dependent on the currently active mode on the specific channel. This register is write-only.

Table 6: IDR register mapping

7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

- COVFS – Disable Counter Overflow Interrupt
- LOVRS - Disable Load Overrun Interrupt (if Wave=0)
- CPAS – Disable RA Compare Interrupt (if Wave=1)
- CPBS – Disable RB Compare Interrupt (if Wave=1)
- CPCS – Disable RC Compare Interrupt
- LDRAS – Disable RA Loading Interrupt (if Wave=0)
- LDRBS – Disable RB Loading Interrupt (if Wave=0)
- ETRGS – Disable External Trigger Interrupt

3.3.3 Interrupt Mask Register

While the Interrupt Enable Register and Interrupt Disable Register is used to turn on or off interrupts, the Interrupt Mask Register contains information whether the interrupt source is enabled or enabled. Each bit in the Interrupt Mask Register (IMR) corresponds to an individual interrupt source. If the bit is set, the interrupt source is enabled, disabled otherwise. This register is read-only.

Table 7: IDR register mapping

7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

- COVFS –Counter Overflow Interrupt
- LOVRS - Load Overrun Interrupt (if Wave=0)
- CPAS –RA Compare Interrupt (if Wave=1)
- CPBS –Compare Interrupt (if Wave=1)
- CPCS –RC Compare Interrupt
- LDRAS –RA Loading Interrupt (if Wave=0)
- LDRBS –RB Loading Interrupt (if Wave=0)
- ETRGS –External Trigger Interrupt

4 Package information

Included with the application note is a driver package. This package contains drivers for the Timer/Counter Module, example code and documentation.

4.1 Drivers

Drivers are available in the package. These drivers are written to be independent of a specific compiler and are successfully tested on gcc and IAR Embedded Workbench®.

4.2 Examples

Examples are available from the corresponding driver package. All functionality is divided into libraries and an example that utilizes the library. There are examples for both generating waveforms and for capturing.

4.3 Documentation

Function specific documentation is available in the package. Refer to readme.html in the source code directory.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature